EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	39	(memory and (register or buffer) and read$4 and writ$4 and image and control$4 and line and clock). clm.	US-PGPUB	OR	ON	2007/11/13 10:52
L2	4	(memory and image and buffer and line and bits and writ$4 and chip and enabl$3 and output$4 and control$3).clm.	US-PGPUB	OR	ON	2007/11/13 10:59
L3	71	(Sang-Hyun near2 Park or Jong-Sik near1 Jeong or Yeon-Cheol near1 Lee or Kang-ju near1 Kim or Hyung-Man near1 Park or Boo-Dong near1 Kwak).in.	US-PGPUB; USPAT; JPO	OR	ON	2007/11/13 10:59

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S36	62054	"382"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:42
S35	131404	"348"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:42
S1	178	348/280.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:42
S37	55141	"358"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:43
S38	15533	"377"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:44
S39	80113	"365"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:45
S40	47296	buffer$3 same read$3 same writ$4 same control$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:46
S41	34298	(memory or RAM or DRAM) same S40	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:47
S44	478	S43 and (S35 or S36 or S37 or S38 or S39)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:48

EAST Search History

S43	984	S41 and S42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:48
S42	41580	image same (interpolat$3 or demosaic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 11:48
S45	150125	line near3 (buffer or memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 14:38
S46	2660	S45 same (interpolat$3 or demosaic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 14:39
S49	118	S48 same image	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 14:41
S48	296	S46 same bit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 14:41
S47	2045	S46 and image	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/11 14:41
S53	96	S51 and (image or video)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:35
S52	0	S51 and 348/231.$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:35
S51	305	bandwidth same S50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:35

EAST Search History

S50	28160	memory near2 control$4 with lines	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:40
S54	2311	(memory or DMA) near2 control$4 with lines with image	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:41
S55	558	S54 and imag$3 near2 sens$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:42
S56	188	S55 and "348"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/08 10:43
L1	39	(memory and (register or buffer) and read$4 and writ$4 and image and control$4 and line and clock). clm.	US-PGPUB	OR	ON	2007/11/13 10:52
L3	71	(Sang-Hyun near2 Park or Jong-Sik near1 Jeong or Yeon-Cheol near1 Lee or Kang-ju near1 Kim or Hyung-Man near1 Park or Boo-Dong near1 Kwak).in.	US-PGPUB; USPAT; JPO	OR	ON	2007/11/13 10:59
L2	4	(memory and image and buffer and line and bits and writ$4 and chip and enabl$3 and output$4 and control$3).clm.	US-PGPUB	OR	ON	2007/11/13 10:59

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memory control line image register buffer inter Search Advanced Search Preferences

Web Results **1** - **10** of about **213,000** for **memory control line image register buffer interpolation read write clock**. (**0.35** seco

Image processing apparatus and **image** processing method employing ...
The **image** processing method as in claim 1 further including the steps of: storing the pixel data in a **memory** in synchronization with a **write clock**; ...
www.freepatentson**line**.com/20010028750.html - 37k - Cached - Similar pages

Line buffer and method of providing **line** data for color ...
A **memory** providing apparatus for an **image** data **interpolation** in an **image** ... the **read** first **line image** data in a prior data area of the **buffer register**, ...
www.freepatentson**line**.com/20040263650.html - 54k - Cached - Similar pages
[More results from www.freepatentsonline.com]

Electronic camera having dual clocked **line memory** - US Patent 6593967
FIFO **memory** in which number of bits subject to each data **read/write** ... **Clock control** circuit with independent timing adjustments for **image** sensing devices ...
www.patentstorm.us/patents/6593967-description.html - 31k - Cached - Similar pages

Memory for video signals - US Patent 5027204
This requirement in itself already makes it clear which elaborate **write-read** devices and their **control** are required if an exclusively random access **memory** ...
www.patentstorm.us/patents/5027204-description.html - 29k - Cached - Similar pages
[More results from www.patentstorm.us]

Multimedia LSI Accelerator with Embedded DRAM
In **image** scaling, **interpolation** from adjacent data in the original **image** .... The **read** and **write control** logic uses RAS and CAS signals just like a standard ...
doi.ieeecomputersociety.org/10.1109/40.641596 - Similar pages

M LSI A E DRAM
of this **memory** specification. The **read** and **write control** logic uses RAS and CAS signals .... command **register**, and the SRC/**image register**. The com- ...
ieeexplore.ieee.org/iel3/40/13937/00641596.pdf?arnumber=641596 - Similar pages

Development of picture converting system applying an NTSC signal ...
Field **Memory** whose **write-clock** is made by the first. PLL and whose **read-clock** is this reference .... each **interpolated line** is the same as one of the **read-** ...
ieeexplore.ieee.org/iel1/30/4057/00156701.pdf?arnumber=156701 - Similar pages
[More results from ieeexplore.ieee.org]

[PDF] AN373: Avalon Video Input Module Application Note
File Format: PDF/Adobe Acrobat - View as HTML
Avalon direct **memory** access (DMA) master to **write image**(s) to. frame **buffer memory**.
■. Avalon **register** slave for **control** and status. Functional ...
www.altera.com/literature/an/an373.pdf - Similar pages

Programmable Logic DesignLine | How to implement a digital ...
The chip includes the digital logic (sample **buffer memory interpolating** digital trigger logic, ... Low level functions (**read/write** samples/**register** values, ...
www.pldesign**line**.com/190302962;jsessionid=RHZKXSP2PAVESQSNDLQSKHSCJUNN2JVN?printableArticle=true - 50k - Cached - Similar pages

(WO/1991/013396) **MEMORY** BASED **LINE**-DELAY ARCHITECTURE
The **read** enable lines and **write** enable lines address each of the **memory** cells .... The

shift **register** outputs change on the rising edge of the **clock** i.e., ...
www.wipo.int/pctdb/en/wo.jsp?WO=1991%2F13396&IA=WO1991%
2F13396&DISPLAY=DESC - 38k - Cached - Similar pages

1 2 3 4 5 6 7 8 9 10 **Next**

Web Results **11** - **20** of about **213,000** for **memory control line image register buffer interpolation read write clock**. (**0.17** sec

EP79542 Gen european software patent - Two-dimensional digital ...
Following output from the first **line buffer**, **interpolated** data lines are .... enable gates 74 and 76, **control** the **read** or **write** modes of **line** buffers 70 and ...
gauss.ffii.org/PatentView/EP79542 - 55k - Cached - Similar pages

EP550229 Gold european software patent - Television screen aspect ...
Meanwhile, since the **write clock** of the field **memory** FF3 is (5/4)fs which is the same as the **read clock** of the **line** memories FF1 and FF2, and its **read clock** ...
gauss.ffii.org/PatentView/EP550229 - 46k - Cached - Similar pages
[More results from gauss.ffii.org]

fpgacpu.org - 3-D Rendering Acceleration
The inner loop (one scan **line**) of this simple polygon rendering algorithm ... easier to do separate **read** and **write** passes on the Z-**buffer memory**, pipelined, ...
www.fpgacpu.org/usenet/render.html - 10k - Cached - Similar pages

[Paper] Streaming Scratchpad **Memory** Organization for Video ...
ALUACU RAM ROMSAD Communication Bus/Network 32b 32b **Image memory** scratchpad scratchpad ..... For the case of pixel-**line** based imple- mentation, **read/write** ...
www.actapress.com/PDFViewer.aspx?paperId=18452 - Similar pages

Leslie Kohn and Neal Margulis Intel Corporation Santa Clara, CA ...
pin to **control** cachability of each **line**'s **read** miss. Each cachable **read** miss results in four bus ... the **write buffer** carries out the actual **memory write**. ...
portal.acm.org/ft_gateway.cfm?id=76313&type=pdf&dl=GUIDE&dl=ACM - Similar pages

BeebEm Change History ========== Version 3.7 (Jon Welch ...
Added ability to pass name of disc **image** on command **line** to run it automatically. ...
Almost full 1770 FDC Support (**read/write** track (format) and force ...
www.mikebuk.dsl.pipex.com/beebem/CHANGES.txt - 22k - Cached - Similar pages

The Truga001: A Scalable Rendering Processor
By generating a **memory control** signal in response to a **write-read** request from .... The Truga001 chip uses a 384-**line** as a frame **buffer** bus and supports a ...
doi.ieeecomputersociety.org/10.1109/38.656790 - Similar pages

[PDF] Specification for TV-8532A CIF/QVGA RESOLUTION COLOR CMOS USB ...
File Format: PDF/Adobe Acrobat - View as HTML
Image. Sensor. 5X Proprietary. Compression. **Line Buffer** ..... **Register** 58 = **Write** desired bit values for outputs, **Read** bit values for inputs ...
mxhaard.free.fr/spca50x/Doc/TransVision/tv_8532a.pdf - Similar pages

[PPT] 2006-11-14 John Lazzaro (www.cs.berkeley.edu/~lazzaro) CS 152 ...
File Format: Microsoft Powerpoint - View as HTML
Control logic sends "this frame". out of other **buffer** to display. .... (**Read/Write**). **Register** R0 is. pixel fragment,. ready for output merge ...
inst.eecs.berkeley.edu/~cs152/fa06/ppt/lec12-1.ppt - Similar pages

Atari Jaguar II - Wikipedia, the free encyclopedia
The display was built in a local **line buffer** from multiple bit-maps, ... blitter and object processor could both **write** and **read** pixels at 66 Mpixels/second. ...
en.wikipedia.org/wiki/Atari_Jaguar_II - 35k - Cached - Similar pages

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memory control line image register b Search

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Web Results **21** - **30** of about **213,000** for **memory control line image register buffer interpolation read write clock**. (**0.14** sec

PTO Manual of Classification for US patents
Including velocity or acceleration **control** 474.31 ....**Interpolation** 474.32 . ..... **Memory** controller (238.4) .**Line** adapter/modem (238.5) .**Buffer** structure ...
www.ibiblio.org/patents/class/CLASS364.html - 67k - Cached - Similar pages

The UltraSPARC Processor -- Technology White Paper
The **register read** may be bypassed if needed operands are contained in the pipeline. .... main **memory**, **control** space, and all external system resources. ...
www.eng.dmu.ac.uk/~pdn/UltraSPARC/ultra_arch_architecture.html - 29k - Cached - Similar pages

A method of affine transformation for rectangular video **image**
Since the subimage is a square, the **control** of **memory** ..... alternating the **read** and **write** for each horizontal scanning, ...
doi.wiley.com/10.1002/(SICI)1520-684X(200007)31:7%3C75::AID-SCJ9%3E3.3.CO%3B2-G - Similar pages

Microprocessors and Microsystems : Configurable implementation of ...
Then, the **interpolated image** is sampled. In practical implementations ..... Each **memory** module is capable of simultaneous **read** and **write** operations. ...
linkinghub.elsevier.com/retrieve/pii/S0141933106001463 - Similar pages

A million transistor systolic array graphics engine
buffer memory for storing the color of each pixel. The. pixels stored in the frame **buffer** are ... which have **read**-modify-**write** cycle times of 250 nsec. ...
www.springerlink.com/index/G173570491505822.pdf - Similar pages

Design of a Parallel Accelerator for Volume Rendering
1: **Control** flow in an ISA. Every processor has **read** and **write** access to its own **memory**. Besides that, it has a. designated communication **register** ...
www.springerlink.com/index/62CA3MN62X9WD3GY.pdf - Similar pages
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(WO/1986/007164) LASER DISPLAY SYSTEM
R/W = **Write** R/W = **Read**. FF7C MSB **Buffer Register** Timer #2 Counter ... The **control** bit associated with the second of the parallel **buffer memory** can be used ...
www.wipo.int/pctdb/en/wo.jsp?WO=1986%2F07164&IA=WO1986%2F07164&DISPLAY=DESC - 37k - Cached - Similar pages

MATLAB Reference (by Category)
Toolbox/**Control** System. dskdemo - Build controller for a disk **read/write** head. ... spline **interpolation**. spldems - Set up Spline command **line** demos. ...
www.glue.umd.edu/~nsw/ench250/reftopic.htm - 77k - Cached - Similar pages

ISSCC '99 Digest of Technical Papers and Slide Supplement
2.2, A Trellis-Coded E 2 PRML Digital **Read/Write** Channel IC ... 6.4, Multi-Phase Driven Split Word-**Line**-Ferroelectric **Memory** Without Plate **Line** ...
128.100.10.145/isscc/1999/digest/MidIndex.htm - 46k - Cached - Similar pages

[PDF] Video and **Image** Processing Up Conversion Example Design

File Format: PDF/Adobe Acrobat - View as HTML
image up to 1024×768 using bicubic **interpolation**. Triple **Buffer** Component ..... **read** and **write** master ports. In the example design, the RAM model is ...

www.altera.com/literature/an/an427.pdf - Similar pages

Previous 1 2 3 4 5 6 7 8 9 10 11 12 **Next**

Web Results **31** - **40** of about **179,000** for **memory control line image register buffer interpolation read write clock**. (**0.67** sec

Patent Number 4907282 Issue Date 1990 03 06 Appl. Data 296852 1989 ...
Character data corresponding to a current display pixel is also **read** from a display **memory**. Then **buffer** data which relates to a current scan **line** and the ...
lpf.ai.mit.edu/Patents/abstracts/395150.1990-1992 - 72k - Cached - Similar pages

ISSCC '99 Digest of Technical Papers and Slide Supplement
2.2, A Trellis-Coded E 2 PRML Digital **Read/Write** Channel IC ... 6.4, Multi-Phase Driven Split Word-**Line**-Ferroelectric **Memory** Without Plate **Line** ...
128.100.10.145/isscc/1999/digest/MidIndex.htm - 46k - Cached - Similar pages

United States Patent: 5841863
Read/write control signals and multi-bit address signals are supplied to the ..... The implementation requires only that the present one-**line memory** (RAM) ...
www.snake.ne.jp/.../380/240&RS=CCL/380/240 - 112k - Cached - Similar pages

[PDF] INTERFFACE **CONTROL** DOCUMENT
File Format: PDF/Adobe Acrobat - View as HTML
The **Memory** Data **Register** contains the **Memory** Data field. This **register** is used to **read** or **write** SRAM. data at the current address in the **Memory** Interface ...
www.thermal-eye.com/Upload/files/manuals/ICD%202000B.pdf - Similar pages

[PDF] OKI Semiconductor ML87V3116 Preliminary
File Format: PDF/Adobe Acrobat
This **memory buffer** stores video input data, display data and other **image** data. ..... Cb/Cr **interpolation** method, 1 bit (**write/read**) ...
www.okisemi.com/eu/docbox/PEDL87V3116-02_2004Sep21.pdf - Similar pages

[PS] (PxFl Texture)
File Format: Adobe PostScript - View as Text
communication **buffer** are configured by software. The **image**- ... required to **read** and **write** SDRAM memories and contain internal ...
www.cs.unc.edu/~molnar/Papers/PxFlTexture.ps - Similar pages

A scalable high-performance graphics processor: GVIP
ent ways in which pixel arrays can **read/write**. to/from the frame **buffer**: horizontal (x), ... and four-**line interpolation** is used is shown in. Fig. 10. ...
www.springerlink.com/index/M77920925141354P.pdf - Similar pages

BABEL: A Glossary of Computer Related Abbreviations and Acronyms
ORI Original (file name extension) OROM Optical **Read**-Only **Memory** ORS Output Record ..... R/W **Read/Write** RWM **Read-Write Memory** RX Receiver RXD Receive Data ...
www.geocities.com/Heartland/Plains/4142/acronyms.htm - 155k - Cached - Similar pages

[PDF] 983X SDG CoverPage.fm
File Format: PDF/Adobe Acrobat - View as HTML
Registers 4 and 5 (DataPort Address and **Read/Write** Select) ... The lower 6 bits of this **register control** the Master **Clock** to most of the scanner. ...
scanjet2200c.sourceforge.net/docs/983x_sdg_all.pdf - Similar pages

0018-8646/98/$3.00 (C) 1998 IBM Recent IBM patents The following ...
... bus turnaround on consecutive **read** and **write** tenures 5640526 L. H. Moulton III, ... determined by shadow **register** address **buffer** 5640586 G. G. Pechanek, ...
www.research.ibm.com/journal/rd/421/patents.txt - 54k - Cached - Similar pages

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